REMARKS

Some typographic corrections have been introduced as amendments. Some of the rejected claims have been amended. No new matter has been added.

Applicant notes that a supplemental Information Disclosure Statement was filed on April 3, 2001, and respectfully requests that such IDS be made of record and considered in the examination of this applicaiton.

Applicant submits this Amendment "D" and Response for the Examiner's consideration. Reexamination and reconsideration of the application, as amended, in view of the following remarks are respectfully requested.

1. STATUS OF THE CLAIMS

Claims 1-28 and 36-63 were presented for examination and they stand rejected and pending in the application. All the pending claims stand rejected under 35 U.S.C. § 103(a). Some of the claims are amended and rejection grounds are traversed below.

2. RESPONSE TO REJECTIONS

2.1. *Claim Rejections Under 35 U.S.C. § 103(a)*

All the pending claims stand rejected under 35 U.S.C. § 103(a) either in view of Xu, *et al.*, U.S. Pat. No. 5,668,055 (hereinafter "Xu") or in view of Xu in combination with one of the following patents: Fiordalice, *et al.*, U.S. Pat. No. 5,420,072 (hereinafter "Fiordalice"), and Schacham-Diamand, *et al.*, U.S. Pat. No. 5,824,599 (hereinafter "Schacham").

As reasoned below, the present method claims recite steps that are not taught or suggested by Xu, that refer to structurally different elements, and that include the selection of materials

according to criteria that are neither taught nor suggested by Xu. Furthermore, neither Fiordalice nor Schacham provide any basis that would overcome the limitations and differences established with respect to the disclosure in Xu. Even if Xu were combined with Fiordalice or Schacham, the combination would not teach or suggest the method recited in any of the present claims; therefore, the cited references, whether alone or in combination, may not render the subject matter recited in the present claims obvious.

Xu discloses the extrusion of a compressibly stressed patternable metal layer 30 under the constrain of a restraining overlying tensile-stressed cap layer 40. Furthermore, the compressibly stressed patternable metal layer 30 in Xu is deposited only partially on barrier layer 20. As reasoned below, Xu is patentably distinguishable from the present method claims and Xu does not teach or suggest the presently recited methods, which are distinguishable from the teachings in Xu on at least the following grounds (1)-(9).

(1) Xu discloses the formation of compressibly stressed patternable metal layer 30. The physical characteristic of being compressibly stressed is required in Xu for the subsequent extrusion process of the material in such layer into recessed spaces. *See, e.g.*, Xu, Fig. 5, second block from the top, col. 2, *ll.* 28-29, col. 4, *ll.* 11-13, 23-24, col. 5, *ll.* 4-10, col. 6, *ll.* 16-17, 35-36, 67, col. 7, *ll.* 1-3, col. 8, *ll.* 30-31. This layer is generally flat and horizontal thus accommodating a stress to be relieved in a subsequent extrusion process. *See, e.g.*, Xu, Figs. 2-3. Therefore, Xu does not teach or disclose the formation of a layer of conductive material such as that recited in the present claims that extends over the seed layer, not only on the flat and horizontal portions of the seed layer, but also on the seed layer within the recessed areas. The teachings in Xu require the formation of a compressibly stressed layer, and it does not follow from the teachings in Xu how one could

implement these teachings to form the electrically conductive layer with the characteristics recited in the present claims to fill the recesses and any void.

(2) Xu discloses the formation of cap layer 40 in tensile stress to restrain upward displacement of patternable metal layer 30 upon extrusion. This physical condition of tensile stress in cap layer 40 is required in Xu. *See, e.g.*, Xu, Fig. 5, third block from the top, col. 2, *ll.* 30-31, 34-38, col. 6, *ll.* 21-36, 45-48, col. 7, *ll.* 40-48, col. 8, *ll.* 33-34. In contrast, an energy absorbing layer is formed on the electrically conductive layer as recited in the present claims. Xu does not teach or suggest the formation of an energy absorbing layer in terms of characteristics and functions that are neither disclosed nor suggested in Xu.

(3) Xu discloses the formation of compressibly stressed patternable metal layer 30 on the portions of barrier layer 20 that do not extend significantly into recesses 14, 16. *See, e.g.*, Xu, Figs. 2-3, col. 4, *ll.* 16-20. In contrast, independent claims 1, 16, 23, 24, 28, 36, 45, and 48 recite the formation of a layer of electrically conductive material on the seed layer including the portions of the seed layer within the recess; independent claims 46 and 54 recite the filling of the recess with an electrically conductive material; and independent claims 57 and 62 recite the formation of an electrically conductive layer on the seed layer extending to terminate at the planar top surface of the dielectric material and the formation of a layer of electrically conductive material on the seed layer including the portions of the seed layer within the recess. These recitations are incorporated in relevant part into dependent claims 2-15, 17-22, 25-27, 37-44, 47, 49-53, 55-56, 58-61, and 63 that depend from these independent claims. The extent, coverage and structural characteristics of the metal layer disclosed in Xu and those of the electrically conductive layer recited in the present method claims are thus completely different.

(4) The materials in Xu are selected for an extrusive process according to physical characteristics that are different from those recited in the material selection of the present claims. In particular, the materials are selected according to Xu in terms of their tensile stress and compressive stress, in addition to electrical conductivity. *See, e.g.*, Xu, col. 2, *ll.* 34-38, col. 4, *ll.* 22-24, col. 5, *ll.* 4-15, 40-43, col. 6, *ll.* 17-19, 27-36, 44-60. In contrast, the present claims recite material selection for different layers in terms of melting points, thermal absorption capacities, thermal insulation capacity, in addition to electrical conductivity. Xu does not teach or suggest any relationship that would permit the interconversion of such different physical properties. Accordingly, Xu does not teach or suggest how to perform the material selections recited in the present claims.

(5) Xu discloses the filling of recesses by an extrusive process that relies on the layer stresses that are built upon their formation. These substantially empty recesses are thus filled with electrically conductive material according to Xu upon heating and extrusion. *See, e.g.*, Xu, Figs. 2-3, col. 4, *ll.* 17-21, col. 7, *ll.* 45-48. In contrast, the present claims recite the formation of electrically conductive material into the recesses before any heating is applied. Therefore, Xu does not teach or suggest the presently claimed methods. Furthermore, the requirements for the stress build-up and maintenance until extrusion and the extrusive process disclosed in Xu seem to be requirements that would discourage one of ordinary skill in the art to pursue the steps recited in the present claims which, as indicated above, recite the formation of electrically conductive material on the seed layer even within the region inside the recesses.

(6) The Office Action assigns to some of the layers disclosed in Xu physical properties, such as that of the energy absorbing layer, recited in the present claims. Applicant notes that this assignment does not follow from any teaching or suggestion in Xu. Furthermore, as noted above,

Xu does not teach or suggest the reliance on properties and physical characteristics such as those recited in the present claims for the purpose of achieving the results of the presently claimed methods. Therefore, even if materials utilized in the method disclosed in Xu have some of the properties recited in the present claims, this fact, in light of the absence of the relevant teachings in Xu, may not be part of an analysis of the present claims under 35 U.S.C. § 103(a). Accordingly, Applicant respectfully traverses these assignments in the Office Action in the context of an analysis under 35 U.S.C. § 103(a) and makes this traversal extensive to the assertions in the Office Action that Xu discloses energy absorbing layer materials. As reasoned above, Xu does not disclose method steps that rely on energy absorbing properties of layered materials as recited in the present claims.

(7) The Office Action indicates that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the diffusion barrier layer in Xu as two sequentially deposited layers composed of the same material since separating what was once one layer, into many layers, involves only routine skill in the art." Office Action, p. 3, second full paragraph. *See also* Office Action, p. 6, ¶ 2.

Applicant respectfully traverses this assertion. Furthermore, this traversal is made extensive to the assertions in the Office Action that Xu discloses barrier layer materials and seed layer materials. As admitted in the Office Action (p. 3), Xu does not disclose or suggest the formation of a barrier layer and a seed layer. The characteristics, features, and advantages of forming a seed layer and a barrier layer do not follow from the teachings of Xu and they are not suggested in the cited references. In contrast, the present application describes characteristics, features and advantages of such multi-layer formation that show that their formation in the context of the presently claimed is not merely the practice of routine practice in the art. *See, e.g.*, Application, pp. 9-10. To the extent that the foregoing characterization of the formation of the seed and barrier layers

in the Office Action is intended to be re-asserted, Applicant respectfully requests that such characterization be accompanied of supporting prior art.

(8) The Office Action asserts that Xu discloses a recess that has an aspect ratio greater than about 4:1. To support this assertion, the Office Action cites "column 2, line 66 - column 8, line 17". Applicant notes that column 2, line 66 is the beginning of the detailed description of the invention in Xu, and that column 8, line 17, is the point at which the last two paragraphs of the detailed description of the invention in Xu begin. This portion of text extends over four out of the four pages that contain the written description in Xu. Accordingly, the Office Action does not point out with specificity a cite that would support the assertion that Xu discloses such recesses. Applicant further notes that Xu refers to a diameter for recesses 14 and 16 of about 2500Å. Xu, col. 4, *ll.* 44-45. These recesses are covered by barrier layer 20, which has a thickness between 150Å and 300Å. Xu, col. 3, *l.* 62, col. 4, *l.* 2. Therefore, the space filled by metal 30 in Xu has a diameter between (2500 - (2x150) =) 2200Å and (2500 - (2x300) =) 1900Å. Applicant has not found a description in Xu of the height of recesses 14 and 16. If such height compares with the height (thickness) of layer 30, this thickness is given as being about 6000Å. Accordingly, an approximate ratio is not more than 6000/1900, which is about 3.15, a number that is significantly less than 4 as obtained from the ratio 4:1. Therefore, Applicant respectfully submits that the assertion that Xu discloses a ratio of 4:1 is not supported in Xu, and that, if anything, Xu discloses ratios smaller significantly smaller than 4:1. To the extent that the foregoing assertion with respect to the aspect ratio disclosed in Xu is intended to be re-asserted, Applicant respectfully requests that such assertion be accompanied with a specific cite to Xu that points out with particularity that the recesses disclosed in Xu have an aspect ratio greater than 4:1.

(9) The reasoning set forth above in items (6) and (8) is herein applied to respectfully traverse the assertion in the Office Action regarding claims 16, 23, and 27. Office Action, p. 5, fifth and sixth full paragraphs.

At least for the reasons set forth above, Xu does not teach or suggest the presently claimed methods with their limitations. Because "the prior art reference (or references when combined) must teach or suggest all the claim limitations", the cited prior art may not establish a *prima facie* case of obviousness. M.P.E.P. §§ 2142-43, 2143.03, pp. 2100-97, 2100-100, 7th ed. (Rev. 1, Feb. 2000) (listing three basic criteria that must be met to establish a *prima facie* case of obviousness).

An additional criterion that must be met to establish a *prima facie* case of obviousness is that there must be some suggestion or motivation in the prior art to modify the reference or to combine reference teachings. *See* M.P.E.P. §§ 2142-43, p. 2100-97, 7th ed. (Rev. 1, Feb. 2000). This criterion is not satisfied because Xu discloses a methodology that relies on extrusion of a compressibly stressed metal layer under the constrain of a restraining overlying tensile stressed cap layer, and at lest one of such layers is formed in a configuration that is different from that of the presently recited electrically conductive layer. Xu addresses recess filling in terms of different problems and provides different methodology to achieve such filling. For the same reasons, Xu does not provide any indication of a reasonable expectation of success for the method steps recited in the present claims, but the provision of this expectation is another requirement that must be satisfied to establish a *prima facie* case of obviousness. *See* M.P.E.P. §§ 2142-43, p. 2100-97, 7th ed. (Rev. 1, Feb. 2000). Furthermore, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." M.P.E.P. §§ 2142-43, p. 2100-97, 7th ed. (Rev. 1, Feb. 2000) (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991)).

As shown above, the present claims recite electrically conductive material that is deposited on the seed layer even within the recess. To achieve this effect, generally horizontal and compressibly stressed layer 30 in Xu would have to be deposited inside recesses 14 and 16, contrary to what is disclosed in Xu. It is well established that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious". M.P.E.P. § 2143.01, p. 2100-99, 7th ed. (Rev. 1, Feb. 2000).

Claims 2, 5-6 that stand rejected under 35 U.S.C. § 103(a) in view of Xu as applied to claim 1 in combination with Fiordalice, depend on independent claim 1. Applicant incorporates herein the cites, quotes and reasoning set forth in the foregoing analysis with respect to Xu. It has not been established that Fiordalice overcomes the differences and limitations set forth above with respect to Xu and the presently claimed methods. Furthermore, Fiordalice does not actually teach or suggest the layering in the recess as recited in claim 1. The TiN layer 24 in Fiordalice is formed on the lower seed layer 22. *See*, Fiordalice, col. 3, *ll.* 60-62. In contrast, the method recited in claim 1 refers to a seed layer on a diffusion barrier layer. Therefore, Xu or Xu in combination with Fiordalice, even if they could be combined, may not render such claims obvious.

Claims 15, 22, 24-28, 46, 47, and 54-63 stand rejected under 35 U.S.C. § 103(a) in view of Xu as applied to the claims above in combination with Schacham. Applicant incorporates herein the cites, quotes and reasoning set forth in the foregoing analysis with respect to Xu. It has not been established that Schacham overcomes the differences and limitations set forth above with respect to Xu and the presently claimed methods. In addition, Schacham fails to teach or suggested the presently recited methods for at least the following reasons.

Schacham discloses the formation of an adhesion promoter layer 16b on a dielectric material 12a, the formation of a barrier layer 17b on the adhesion promoter layer 16b, and the formation of a seed layer 18b on the barrier layer 17b. *See, e.g.*, Schacham, Fig. 19. Schacham does not teach or suggest the formation of the diffusion barrier layer without such adhesion promoter layer.

In addition, the diffusion barrier layer, the seed layer, and the electrically conductive layer in the present claims comprise materials whose melting points satisfy the specific relationships. This is in contrast also with the materials recited in Schacham, which generally do not satisfy the limitations recited in claim 57 regarding the melting points. For example, Schacham discloses that the barrier layer can be formed from Ti (melting point 1660°C ± 10°C) and that the seed layer can be formed from Pt (melting point 1772°C) or Rh (melting point 1966°C ± 3°C). *See*, Schacham, col. 7, *ll.* 22-31. Clearly, these melting points do not satisfy the recited relationship, according to which the diffusion barrier layer material has a melting point greater than or equal to that of a material from which the seed layer is composed. Furthermore, Schacham discloses that a seed layer can be formed from Ag (melting point 961.93°C) or Au (melting point 1064.43°C) and that the conductor layer can be Cu (melting point 1083.4°C ± 0.2°C). *See*, Schacham, col. 7, *ll.* 22-31. Clearly, these melting points do not satisfy the recited relationship, according to which the material from which the seed layer is composed has a melting point greater than or equal to that of the electrically conductive layer material. Therefore, Schacham discloses the formation of layered materials of melting point characteristics that do not correspond with those recited in the present claims, and Schacham relies on an adhesion promoter layer that is not part of the recitation in the present claims. It has not been shown how this disclosure teaches in light of the ordinary skill in the art the formation of specific layers with materials that satisfy the melting point relationships recited in these claims.

Furthermore, Applicant notes that Xu and Schacham are not combinable as in the Office Action (pp. 8-9) because neither Xu nor Schacham provide any teaching or suggestion that the methodology disclosed in Xu would be applicable to the formation of the structure disclosed in Schacham or vice-versa. Instead, Applicant submits that the modifications that would have to be introduced to such effect are neither taught nor suggested by any one of such references, and that it is not shown either that such modifications would lead to a successful result.

Therefore, Xu or Xu in combination with Schacham, even if they could be combined, may not render such claims obvious.

Applicant finally notes that the Office Action in a number of instances selects specific individual features recited in the claims and characterizes such individual features as being known and involving only routine skill in the art. *See, e.g.*. Office Action, pp. 4-5 (regarding planarization), p. 7, (regarding deposition and fabrication processes), p. 9 (regarding materials). To this respect, and to the extent that this reasoning is intended to be re-asserted, Applicant respectfully notes that this reasoning has clearly been rejected as a legal standard for determining patentability, even when any specific recited limitation is known. For example, the Federal Circuit has stated that "[n]othing in the references alone or in combination suggests the claimed invention as a solution to the problem .... That the claimed invention may employ known principles does not itself establish that the invention would have been obvious." *Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 U.S.P.Q. 481, 488-89. Furthermore, in an analysis under 35 U.S.C. § 103, the relevant inquiry "is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." (Underlining in the original) M.P.E.P. § 2141.02, p. 2100-94, 7th ed. (Rev. 1, Feb. 2000) (citing *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 U.S.P.Q. 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218

U.S.P.Q. 698 (Fed. Cir. 1983)). Therefore, even if, *arguendo*, any presently recited claim limitation were known, the relevant inquiry under 35 U.S.C. § 103 requires the consideration of the claimed invention as a whole and a showing that such claimed matter is obvious, rather than the showing that any number of specific limitations taken individually are known.

Consequently, Applicant respectfully submits that Xu, whether combined or not with Fiordalice or Schacham, does not support a *prima facie* case of obviousness regarding the present claims. Applicant respectfully requests the reconsideration and withdrawal of this rejection.

3. CONCLUSIONS

In view of the above, Applicant respectfully maintains that the present application is in condition for allowance. Reconsideration of the rejections is requested. Allowance of claims 1-28 and 36-63 at an early date is solicited.

In the event that the Examiner finds any remaining impediment to a prompt allowance of this application which could be clarified by a telephonic interview, or which is susceptible to being overcome by means of an Examiner's Amendment, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 8th day of June 2001.

Respectfully submitted,

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Marked up Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(1)(ii):

Applicant submits the following marked up version only for claims being changed by the current amendment, wherein the markings, if any, are shown by brackets (for deleted matter) and/or underlining (for added matter).

1. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

forming a recess within a dielectric material situated on a semiconductor lower substrate, said recess extending below a top surface of said dielectric material;

forming a diffusion barrier layer on the recess within the dielectric material;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

forming an energy absorbing layer on said electrically conductive layer, said energy absorbing layer having a greater thermal absorption capacity than that of said electrically conductive layer;

applying, omnidirectionally, energy to said energy absorbing layer to cause said electrically conductive layer to flow within said recess; and

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

16. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer <u>including the portion of the seed layer within said recess</u>, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed;

heating, omnidirectionally, the energy absorbing layer to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

23. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer <u>including the portion of the seed layer within said recess</u>, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed,

being is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating with a furnace the energy absorbing layer to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

24. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

forming a dielectric material on a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

patterning and etching the dielectric material so as to form a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench being parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer composed of aluminum on the seed layer <u>including the portion of the seed layer within said recess</u>, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum, said energy absorbing layer:

having a greater thermal absorption capacity than that of said layer composed of aluminum; and

being composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the layer composed of aluminum;

heating omnidirectionally with a furnace the energy absorbing layer to cause said layer composed of aluminum to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum that are situated above the top surface of the dielectric material.

28. (Thrice Amended) A method for manufacturing an interconnect structure comprising:

forming at least one silicon layer on a monocrystalline silicon layer of a semiconductor substrate assembly, said silicon layer being selected from the group consisting of undoped silicon dioxide, doped silicon dioxide, undoped silicate glass, and doped silicate glass, wherein said monocrystalline silicon layer defines a plane;

patterning and etching the at least one silicon dioxide layer so as to form a recess therein, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the at least one silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said at least one silicon layer, the trench being parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the at least one silicon layer, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer composed of aluminum on the seed layer <u>including the portion of the seed layer within said recess</u>, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which

the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum, said energy absorbing layer having a greater thermal absorption capacity than that of said layer composed of aluminum and being composed of a material:

having both a higher thermal insulation capacity and electric insulation capacity than aluminum; and

selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating omnidirectionally with a furnace the energy absorbing layer to cause said layer composed of aluminum to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum that are situated above the top surface of the at least one silicon layer.

36. (Twice Amended) A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming an electrically conductive layer on the seed layer <u>including the portion of the seed layer within said recess</u>;

forming upon the electrically conductive layer an energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer;

flowing the electrically conductive layer within the recess by omnidirectionally heating the energy absorbing layer.

37. (Once Amended) The method as defined in Claim 36, wherein the melting point of:

the diffusion barrier layer is not less than that of the seed layer and is greater than that

of the electrically conductive layer; and

the seed layer is not less than that of the electrically conductive layer[;].

45. (Twice Amended) A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming a first layer on the seed layer <u>including the portion of the seed layer within said recess</u>;

forming upon the first layer a second layer that can absorb more heat than the first layer;

heating, omnidirectionally, the first and second layers to flow the first layer within the recess by heat.

48. (Twice Amended) The method as defined in Claim 46, wherein filling the recess with the electrically conductive material further comprises:

forming a diffusion barrier layer in contact with the semiconductor substrate and the dielectric material;

forming a seed layer upon the diffusion barrier layer and composed of a material having a melting point less than that of the material from which the diffusion barrier layer is composed and being selected from a group consisting of ceramics, metallics, and intermetallics;

forming a conductor layer upon the seed layer <u>including the portion of the seed layer within said recess</u>; and

forming an energy absorbing layer on the conductor layer that is composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the conductor layer is composed;

wherein the omnidirectional heating is performed with a furnace.

57. (Twice Amended) A method for manufacturing an interconnect structure, the method comprising:

forming a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

forming a dielectric material on the lower substrate having a planar top surface;

forming a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane said lower substrate;

forming a diffusion barrier layer on the trench and the contact hole;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer <u>within the trench and contact hole</u> and extending to terminate at the planar top surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed; and

applying, omnidirectionally, energy to the electrically conductive layer to cause the electrically conductive layer to flow within the recess.

62. (Twice Amended) A method for manufacturing an interconnect structure, the method comprising:

providing a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

forming a dielectric material on the monocrystalline silicon layer;

forming a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said contact hole being oriented perpendicular to the plane of said monocrystalline silicon layer, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of said monocrystalline silicon layer;

forming a diffusion barrier layer on the trench and the contact hole, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

forming a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer <u>within the trench and the contact hole</u> and extending to terminate at the planar surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is

composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed being selected from the group consisting of aluminum and copper; and

applying, omnidirectionally, energy to the electrically conductive layer to cause the electrically conductive layer to flow within the recess.

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